REMARKS

The Examiner has stated that: this application is in condition for allowance except for the following formal matters." Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner has stated: "the specification is objected to for the reasons listed below. Correction is required. In paragraph [0039], line 6, "110" should read "100". In paragraph [0045], line 8, "320B" should read "320D". In paragraph [0047], line 9, "NFET" should read "PFET". In paragraph [0050], line 9, "NFET" should read "PFET". In paragraph [0051], line 7, "100" should read "110" (see the Figs. 5-6 disclosure). In paragraph [0051], line 7, "high" should read "low" (see the Figs. 5-6 disclosure). In paragraph [0051], line 11, "N3 and N4" should read "N1 and N2". In paragraph [0051], line 11, "high" should read "low". In paragraph [0053], line 9, "NFET" should read "PFET". In paragraph [0054], line 6, "100" should read "110" (see the Figs. 5-6 disclosure). In paragraph [0054], line 7, "high" should read "low" (see the Figs. 5-6 disclosure). In paragraph [0054], line 14, "high" should read "low" (see the Figs. 5-6 disclosure)."

The Examiner has further stated: "claims 1-30 are objected to as explained below. Correction is required. Independent claim is objected to because "first" (line 15) should read "third". Claims 2-14 depend on independent claim 1 and are therefore similarly objected to. Claim 2 is further objected to because "second" (line 3) should read "third". Claim 3 is further objected to because "second" (line 2) should read "third". Independent claim 15 is objected to because "a pass gate transistor" (line 7) should read "a pull down latch transistor". Independent claim 15 is objected to because "a pass gate transistor" (line 11) should read "a pull up latch transistor". Claims 16-28 depend on independent claim 15 and are therefore similarly objected to. Independent claim 29 is objected to because "a

{110} of said fin bodies of said first and second pull up latch transistors" (lines 18-19) should read "a {110} crystal plane, of said fin bodies of said first and second pull up latch transistors". Independent claim 29 is objected to because "crystal planes of said first, second and third fin bodies co-aligned" (lines 25-26) should read "crystal planes of said fin bodies of said pass gate transistors, said pull down latch transistors and said pull up latch transistors". Claim 30 depends on independent claim 29 and is therefore similarly objected to."

In response to the Examiners objections to the specification, Applicants have made all the corrections as indicated except for the following six objections: In paragraph [0051], line 7, "100" should read "110." In paragraph [0051], line 7, "high" should read "low." In paragraph [0051], line 11, "high" should read "low." In paragraph [0054], line 6, "100" should read "110." In paragraph [0054], line 7, "high" should read "low". In paragraph [0054], line 14, "high" should read "low."

Applicants maintain "100" in paragraph [0051], line 7, "high" in paragraph [0051], line 7, "high" in paragraph [0051], line 11, "100" in paragraph [0054], line 6, " high" in paragraph [0054], line 7 and "high" in paragraph [0054], line 14 were intended and properly describe Applicants invention. The Examiner has assumed vertical axis 330A is orientated 22.5° counterclockwise from the {100} crystal plane and 22.5° clockwise from the {110} crystal plane in framing his objections. Applicants believe that the description of FIGs. 9, and 10 in the specification these six objections are based on are correct when vertical axis 330A is orientated 22.5° clockwise from the {100} crystal plane and 22.5° counterclockwise from the {110} crystal plane. It should be noted FIGs. 9, 10, 11 and 12 will not change whichever of these two orientations is assumed because of the silicon crystal plane symmetry rules taught in paragraphs [0020] and [0021]. However, Applicants have amended paragraphs [0051] and [0053] to more

fully clarify the intended orientation of axes 330 and 330A in FIGs. 9, 10, 11 and 12. Applicants believe that this does not add new matter for the reasons given *supra* relative to silicon crystal plane symmetry and in light of Applicants teaching in paragraph [0035] that "FIGs. 6, 8, 9, 10, 11 and 12 as well as FIG. 5 of the present disclosure are based on a <100> substrate having a notch located **+22.5° (or -22.5°)** from the {100} plane and **-22.5° (or +22.5°)** from the {110} plane." This teaching supports either orientation of axes 330 and 330A.

In response to the Examiners objection to claims 1-30, Applicants have amended claims 1-3, 15-17 and 29 to include the Examiners requests.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-30 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is authorized to charge and/or credit Deposit Account No. 09-0456.

Respectfully submitted,
FOR: Anderson et al.

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